Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1.-17. (canceled)

18. (currently amended) A data processing system comprising:

a system controller having:

a first memory channel controller;

a second memory channel controller; and

a high-speed bus arbiter;

an input output (IO) controller coupled to the high-speed bus arbiter via a high speed bus, and having a low-speed bus arbiter, wherein the low-speed arbiter supports a slower bus rate than the high-speed bus arbiter.

19. (previously presented) The system of claim 18, wherein a bus rate of the high-speed bus arbiter is at least 10 percent faster than the bus rate of the low-speed bus arbiter.

20. (previously presented) The system of claim 19, wherein the bus rate of the high-speed bus arbiter is approximately 66 Mbits per second per data pin and the bus rate of the low-speed bus arbiter is approximately 33 Mbits per second per data pin.

21. (canceled)

22. (original) A system comprising:

a first controller having an arbiter to arbitrate requests for a first bus of a predefined protocol type at a first data rate; and

an second controller having:

an arbiter to arbitrate requests for a second bus of the predefined protocol type at a second data rate, wherein the first data rate is at least 10 percent greater than the second data rate; and

control circuitry to interface to the first bus.

23. (previously presented) The system of claim 22, further comprising:

an IO device coupled to the control circuitry of the second controller without being coupled to the arbiter of the first controller.

24. (currently amended) A data processing system comprising:

a system controller having:

a first memory channel controller;

a second memory channel controller;

a high-speed bus arbiter;

an input output (IO) controller coupled to the high-speed bus arbiter <u>via a first high speed bus</u>, and having a low-speed bus arbiter, wherein the low-speed arbiter supports a slower bus rate than the high-speed bus arbiter; and

a data storage device coupled to the IO controller <u>via a second high speed bus</u> to transmit data at a data rate higher than the data rate of the low-speed bus arbiter.